Model 1911A
VXIbus Pulse Generator

Operation Manual

1911A CCN 9302

Manual Assy Part Number: 5585061-03
Manual Text Part Number: 5580098-03
Printed in USA

Warranty

Phase Matrix, Inc. warrants this product to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level is not covered by the warranty. Removal, defacement, or alteration of any serial or inspection label, marking, or seal may void the warranty. Phase Matrix, Inc. will repair or replace, at its option, any components of this product which prove to be defective during the warranty period, provided the entire unit is returned PREPAID to Phase Matrix, Inc or an authorized service facility. In-warranty units will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No warranty other than the above is expressed or implied.

Certification

Phase Matrix, Inc. certifies this instrument to be in conformance with the specifications noted herein at time of shipment from the factory. Phase Matrix, Inc. further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology.

Manual Change Information

As Phase Matrix, Inc. continually improves and updates its products, changes to the material covered by the manual will occur. When a part or assembly in a Phase Matrix, Inc. instrument is changed to the extent that it is no longer interchangeable with the earlier part, the configuration control number (CCN) of the instrument, shown on the title page of the manual, will change, and a new edition of the manual will be published.

To maintain the technical accuracy of the manual, it may be necessary to provide new or additional information with the manual. In these cases, the manual is shipped with a Manual Update. Please be sure to incorporate the information as instructed in the Manual Update.

SAFETY

The Phase Matrix, Inc. Model 1911A is designed and tested according to international safety requirements, but as with all electronic equipment, certain precautions must be observed. This manual contains information, cautions, and warnings that must be followed to prevent the possibility of personal injury and/or damage to the instrument.

SAFETY AND HAZARD SYMBOLS

WARNING
A WARNING denotes a hazard to personnel. It calls attention to a procedure or practice, which, if not correctly performed or adhered to, could result in personal injury.

CAUTION
A CAUTION denotes a hazard to the equipment. It calls attention to an operating procedure or practice, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

This is a general warning that appears whenever care is necessary to prevent damage to the equipment.

Dangerous Voltage

Toxic Substance

Static-Sensitive Component

Fire Hazard

OVERALL SAFETY CONSIDERATIONS

WARNING

Before this instrument is switched on, it's protective earth terminals *must* be connected to the AC power cord's protective conductor. The main plug *must* only be inserted in a socket/outlet that has a protective earth contact. The protective action must not be negated by using an extension cord (power cable) or adapter that does not have a protective earth (grounding) conductor.

WARNING

Use only fuses of the type specified with the required current and voltage ratings. Never use repaired fuses or short-circuited fuse holders, as doing so causes shock and/or fire hazard.

WARNING

Whenever it is likely that electrical protection is impaired, the instrument *must* be made inoperative and be secured against any unintended operation.

WARNING

All protective earth terminals, extension cords, autotransformers, and other devices connected to this instrument *must* be connected to a socket/outlet that has a protective earth contact. Any interruption of the protection causes a potential shock hazard that can result in personal injury.

WARNING

The power supply is energized whenever AC power is connected to this instrument. Disconnect the AC power cord before removing the covers to prevent electrical shock. Internal adjustments or servicing that must be done with the AC power cord connected must be performed only by qualified personnel.

WARNING

Since the power supply filter capacitors may remain charged after the AC power cord is disconnected from the equipment, disconnecting the power cord does not ensure that there is no electrical shock hazard.

WARNING

Some of the components used in this instrument contain resins and other chemicals that give off toxic fumes if burned. Be sure to dispose of these items properly.

WARNING

Beryllia (beryllium oxide) is used in the construction of the YTF assembly. This material, if handled incorrectly, can pose a health hazard. *NEVER* disassemble the microwave counter assembly.

CAUTION

Static sensitive components are used in the YTF Assembly. These components can be damaged if handled incorrectly.

CAUTION

Before connecting power to the instrument, ensure that the correct fuse is installed and the voltage-selection switch on the instrument's rear panel is set properly. Refer to INSTALLATION Section 2, *Installation.*

CAUTION

Excessive signal levels can damage this instrument. To prevent damage, do not exceed the specified damage level. Refer to the instrument specifications in Section 1 of this manual.

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GENERAL INFORMATION

DESCRIPTION

The EIP Model 1911A VXIbus Pulse Generator is a register-based VXI module capable of generating four independent pulse signals over a pulse repetition frequency (PRF) range of 1 Hz to 10 MHz. The PRF, pulse width, pulse delay, signal amplitude, and DC offset are independently settable on each channel. Along with the four output channels, the 1911A provides a front panel input for triggering. Other than interface address switches, the instrument has no manual controls, The 1911A is a VXIbus "C" size, 1-slot plug-in module that requires a VXIbus mainframe and instrument controller for operation.

OPERATING CONDITIONS

The EIP 1911A pulse generator is designed to operate at temperatures from 0 to 55 °C at a relative humidity not to exceed 95% (75% over 25 °C; 45% over 40 °C). The pulse generator will perform to specifications at altitudes not exceeding 10,000 ft (3050 m) and will tolerate vibration not exceeding 2 g. It is fungus resistant. The module housing is not designed to provide protection from severe mechanical shock or liquids and is intended for normal VXIbus use in an environmentally clean area.

The 1911A pulse generator meets the requirements of MIL-T-28800D, Type III, Class 7, Style G, Color R with the following modifications and exceptions:

1. The non-operating temperature requirement is limited to the range of -40 to +71 °C.
2. The operating and non-operating altitude requirements are not invoked.
3. The EMI requirement complies with VXIbus System Specifications Revision 1.3.
4. The warm up time is 5 minutes at 25 °C ambient temperature.

STORAGE

To prevent possible damage to the instrument, it must be stored in an antistatic bag or enclosure and in an environment that is protected from moisture, dust, and other contaminants. Do not expose the instrument to temperatures below -40 °C or above 71 °C, nor to altitudes above 40,000 ft (12,000 m).

SPECIFICATIONS

GENERAL

Operating Temperature Range	0 to 55 °C
Non-operating Temperature Range	-40 to 71 °C
Relative Humidity	0 to 95%, non-condensing
EMI	Complies with VXIbus Revision 1.3/1.4 specifications
Warm-up Time	<5 minutes at 25 °C ambient temperature
Weight	<5 lbs
Connectors	BNC female on front panel

VXIbus

Compatibility	Full compliance with VXIbus Specification 1.3 and 1.4 for register-based instruments
Module Size	C-size, 1 slot wide
Device Type	Register-based instrument
Protocol	Not used
Local Bus	Not used
ECLTRG Utilization	All available
TTLTRG Utilization	All available
CLK10 Utilization	Frequency reference
Cooling	1 mm H_2O @ 1.6 liters/s
Power Dissipation	<82 watts

Current Requirements

Voltage(Vdc)	+5	+12	+24	-2	-5.2	-12	-24
IPEAK (Amps)	6.0	-	1.0	0.5	0.5	-	1.0

OUTPUT

Pulse Width (PW)	
Range	50 ns to 838 ms
Resolution	50 ns
Pulse Delay (PD)	
Range	50 ns to 838 ms
Resolution	1 ns
Accuracy	
1 to 49 ns	±5% ±1 ns
50 ns to 838 ms	Same as VXI CLK10

SPECIFICATIONS (Continued)

OUTPUT (Continued)

Pulse Repetition Frequency (PRF)	
Range	1 Hz to 10 MHz
Resolution	$\left(\frac{50\text{ ns}}{PW+PD}\right)$ x (PW + PD + 50 ns) PD rounded to the nearest 50 ns.
Output Amplitude	
Range 0	0 to 1.05 V p-p into an open circuit 0 to 0.5 V p-p into 50 Ω
Range 1	0 to 10.5 V p-p into an open circuit 0 to 5.25 V p-p into 50 Ω
Output Resolution	
Range 0	0.256 mV typical into an open circuit
Range 1	2.56 mV typical into an open circuit
Output Accuracy	
Range 0	±5% at 1 kHz, 50% duty cycle, 1.05 V p-p
Range 1	±5% at 1 kHz, 50% duty cycle, 10.5 V p-p
Output Offset	0 to ±5 Vdc into an open circuit 0 to ±2.5 Vdc into 50 Ω
Output Offset Resolution	2.44 mV typical
Offset Accuracy	±5% at ±5 Vdc
Amplitude + Offset Level	≤10 V p-p maximum into an open circuit
Logic Sense	True or inverted polarity
Settling Time	<1 ms after channel load command
Transition Time	<20 ns typical, 10 to 90%, 5.0 V p-p into 50 Ω
Output Impedance	50 Ω nominal
Drive Capability	50 Ω
Triggering	
Trigger Sources	Front panel, TTLTRG, or ECLTRG trigger lines
Trigger Uncertainty	50 ns
Channel to Channel Delay	100 ns typical
Trigger Levels	
Front Panel	TTL pulse, 30 ns wide minimum, 10 kΩ
TTLTRG	Pulse, 30 ns wide minimum
ECLTRG	Pulse, 8 ns wide minimum

Note: Specifications subject to change without notice.

ACCESSORIES

011 Extra Operation Manual (one supplied at no charge with each instrument)

DECLARATION OF CONFORMITY

Application Of Council Directive 89/336/EEC

Standards to which Conformity is Declared:

EMC: EN50011
EN50082-1

Standards to which Compliance is Declared:

Safety: IEC 1010-1 (1990)

Manufacturer's Name:	EIP Microwave, Inc.
Manufacturer's Address:	1745 McCandless Drive Milpitas, California 95035
Type of Equipment:	VXIbus Pulse Generator
Model Name(s):	1911A
Tested By:	Rockford Engineering Services, Inc. 9959 Calaveras Road Sunol, CA 94586 USA
Project Engineer:	Mr. Bruce Gordon and Leo Hernandez
Reviewer:	Mr. Michael Gbadebo, P.E.

I, the undersigned, hereby declare that the equipment specified above conforms to Directives and Standards listed.

For: **EIP Microwave**

Name: Pete Pragastis
Title: Manager of Engineering

Signature: _____

Date: 3/26/96

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INSTALLATION

UNPACKING

Before unpacking the instrument, carefully inspect the shipping carton for any signs of damage. If the carton or instrument is damaged, immediately notify shipper's agent. Remove the packing carton and supports, being careful not to scar or damage the instrument. Make a complete visual inspection of the pulse generator, checking for any damage or missing components. Report any problems to EIP immediately. Save the packing material so it can be reused in the event that the instrument needs to be returned to EIP for repair or calibration.

SETTING THE LOGICAL ADDRESS

Before installing the pulse generator in the VXIbus mainframe, set the instrument to the desired logical address between 1 and 254 (decimal). The factory default setting for the logical address is 11 hexadecimal (17 decimal). The logical address of the pulse generator is set using the two rotary-type hexadecimal switches located on the bottom of the module (see Figure 2-1). To set the logical address, dial each switch to the hexadecimal value desired. For example, to set a logical address of 17 hexadecimal (23 decimal), use a small flathead screwdriver (or similar tool), and rotate the MSB switch to 1 and the LSB switch to 7. The logical address desired must be a value between decimal 1 and 254. Logical address 0 is reserved for Slot 0 devices. Logical address 255 is reserved for dynamically configured devices. The EIP 1911A does not support dynamic configuration.

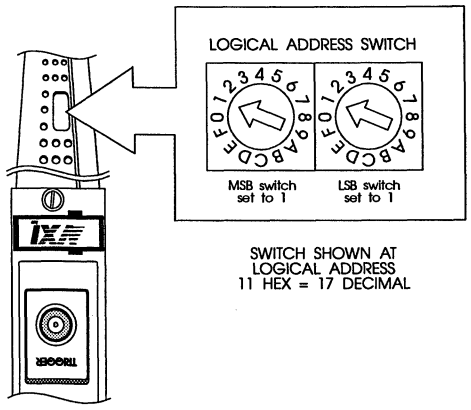

Figure 2-1. Logical Address Switch Locations.

POWER AND COOLING

The EIP 1911A pulse generator operates over an ambient temperature range from 0 to 55 °C and consumes up to 82 watts (see Specifications in Section 1). When configuring your VXIbus system, make sure that the chassis has sufficient power and cooling capacity for the pulse generator along with the other instruments in the chassis. Refer to chassis specifications and cooling capacity curves.

INSTALLATION

The 1911A is a VXIbus module designed to be installed in a VXIbus mainframe. Prior to installing the pulse generator in a VXIbus mainframe, verify that all VXI defined voltages are present and within limits, and make sure the mainframe is capable of supplying the required current (see Specifications in Section 1).

CAUTION

Prior to installing the 1911A in a VXIbus mainframe, verify that all the VXI defined voltages are present and that the mainframe is capable of supplying the required current.

CAUTION

Do not plug pulse generator into VXIbus mainframe with power applied.

The pulse generator is a 1 slot, C-size module that can be installed into any slot of a VXIbus mainframe except slot 0. Slot 0 is reserved for the resource manager. To install the pulse generator into the VXIbus mainframe, first turn mainframe power off. Next, place the pulse generator card edges into the front mainframe guides (top and bottom). Gently slide the pulse generator towards the rear of the mainframe until the connectors just mate with the backplane. Firmly seat the module against the backplane connectors making sure the front panel is flush with the front of the card cage. Tighten down the retaining screws to ensure the module remains fully seated.

CAUTION

Do not use retaining screws to seat module.

INCOMING OPERATIONAL CHECK

A VXIbus mainframe along with a slot 0 resource manager and an instrument controller are required to verify that the pulse generator is operational. Whenever a VXIbus mainframe is energized, the resource manager queries each device checking for proper operation.

IN CASE OF PROBLEMS

In the event that a problem does occur, there are a few things to check prior to returning the instrument for repair.

1. If the unit has never worked in the particular system, the problem may be due to the system and not an instrument fault. In this case, call EIP at the phone number listed on the cover page of the manual and ask for Customer Support.

2. Verify logical address setting on the instrument.

3. Verify that all the VXI specified voltages are present.

SERVICE INFORMATION

PERIODIC MAINTENANCE

No periodic preventive maintenance is required. However, to maintain accuracy, it is recommended that the pulse generator be recalibrated every 12 months or whenever a problem is suspected.

PULSE GENERATOR IDENTIFICATION

This pulse generator is identified by three sets of numbers: the model number (EIP 1911A), serial number, and a configuration control number (CCN). These numbers are located on a label affixed on the side of the module and must be included in any correspondence regarding your pulse generator.

FACTORY SERVICE

If the pulse generator is being returned to EIP for service or repair, be sure to include the following information with the shipment.

- Name and address of owner.
- Model, complete serial number, and CCN of the pulse generator.
- A complete description of the problem. Try to provide enough information so that the problem can be verified, i.e., Under what conditions did the problem occur? Did the unit work and then fail? What other equipment was connected to the pulse generator?
- Name and telephone number of someone familiar with the problem who may be contacted by EIP if any further information is required.
- Shipping address to which the pulse generator is to be returned. Include any special shipping instructions. Pack the pulse generator for shipping as detailed in Shipping Instructions.

SHIPPING INSTRUCTIONS

Place the pulse generator in an antistatic bag or enclosure, wrap in heavy plastic or kraft paper, and repack in the original container, if available. If the original container cannot be used, pack in a heavy (275 pound test) double-walled carton with approximately two inches of packing material between the pulse generator and the inner carton. Seal carton with strong filament tape or strapping. Mark the carton to indicate that it contains a fragile electronic instrument. Ship to the EIP address on the title page of the manual.

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FRONT PANEL

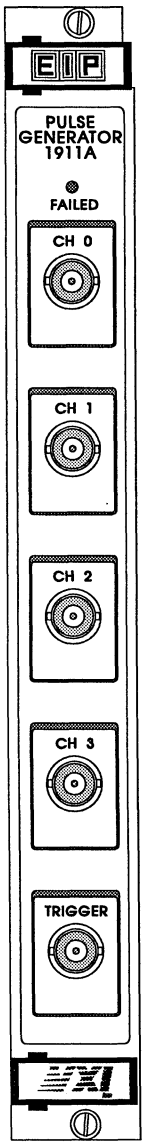

Figure 3-1. Front Panel.

INTRODUCTION

This section describes the functions of the front panel LED and connectors.

FRONT PANEL STATUS LED

The FAILED LED lights to indicate that the pulse generator has failed, or is in the process of executing its self-test. Failures are typically the result of an internal component failure or inadequate power supply current. The FAILED LED follows the condition of the VXIbus SYSFAIL line. If the unit has failed, the LED will remain lit even if SYSFAIL is inhibited by the commander.

FRONT PANEL CONNECTORS

OUTPUT CONNECTORS

The 1911A provides four identical, independently controlled 50 Ω output channels. These are front panel BNC female connectors labeled CH0, CH1, CH2, and CH3.

INPUT CONNECTOR

The 1911A has one front panel input connector; the external TTL trigger BNC input—labeled TRIGGER. The input impedance for the trigger input is 10 kΩ. The 1911A can be triggered externally by applying a TTL pulse, with a pulse width of at least 30 ns. The 1911A triggers on the rising edge of the input pulse.

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PROGRAMMING

The EIP 1911A is a register based A16/A24 VXIbus Pulse Generator. The A16 configuration registers contain basic information about the module including manufacture ID, device type, status/control, and the A24 offset address.

All programming of the 1911A is done by writing to the control registers located in the A24 address space. The function of each register is defined in this section.

A16 BASIC CONFIGURATION REGISTERS

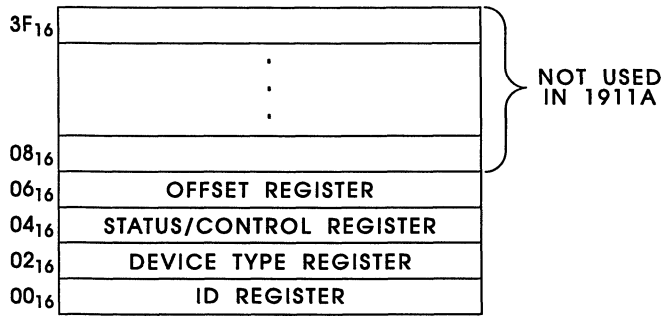


Figure 4-1. 1911A Configuration Registers.

MANUFACTURER ID REGISTER (READ ONLY)

Bits 0 thru 11 of the Manufacturer ID Register contain the manufacture's ID. Bits 12 and 13 establish the address space supported. Bits 14 and 15 establish the device class.

The Manufacturer ID number for EIP is 4008. This number is programmed into bits 0 through 11 of the Manufacturer ID Register and cannot be changed.

EIP Manufacture ID # = 4008 decimal = 1111 1010 1000 binary

The 1911A supports both A16 and A24 addressing modes. Per the VXIbus standard, bits 12 and 13 identify the addressing modes supported by the instrument. For instruments supporting A16/A24 addressing modes, both bits 12 and 13 are zero.

Address Space = A16/A24 ⇒ b12 = 0 and b13 = 0

Per the VXIbus standard, bits 14 and 15 indicate the device class. For register based instruments, both bits 14 and 15 are one.

Device Class = Register Based ⇒ b14 = 1 and b15 = 1

Manufacturer ID Register (b+00h)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Defined															
Read	1	1	0	0	1	1	1	1	1	0	1	0	1	0	0	0
	Device Code			Addressing Mode	Manufacturer ID											

DEVICE TYPE REGISTER (READ ONLY)

Bits 0 thru 11 of the Device Type Register contain the model code for the instrument. For the EIP 1911A the model code is 1911.

Model Code = 1911 decimal = 0111 0111 0111 binary

Bits 12 through 15 of the Device Type Register establish the memory requirements for A16/A24 and A16/A32 devices. The resource manager uses this information when allocating memory for the system.

The following formula is used to determine the contents of bits 12 through 15 based on the memory requirements of the instrument.

$$\text{Required memory} = 256^{a} \times 2^{23-m}$$

where: a = contents of address space field in ID register.
a = 00 for the 1911A.
m = required memory in integer increments of 2^n.
The 1911A needs 1304 bytes, so the allotted memory is 2048 bytes.

$$2^n = 2048 \Rightarrow n = 11$$

$$2^{11} = 2^{(23-12)} \Rightarrow m = 12$$

12 decimal = 1100 binary

Device Type Register (b+02h)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Defined															
Read	1	1	0	0	0	1	1	1	0	1	1	1	0	1	1	1
	Memory Required				Model Code											

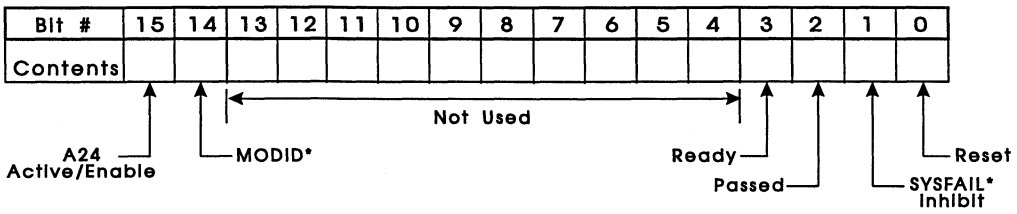
STATUS/CONTROL REGISTER (READ/WRITE)

This register serves a dual function by providing both status information on the 1911A and limited control of the instrument.

The status information is obtained by reading the contents of this register. At power-up, the 1911A goes through an initialization routine and writes a one (1) to bit 3 of the Status Register when the initialization routine is complete. If the 1911A does not detect a problem during the initialization routine, then it writes a one (1) to bit 2 indicating it is ready to begin normal operation. At power-up, the resource manager reads this register to verify that the 1911A has passed initialization and is ready to execute commands.

The resource manager can also write to specific bits in this register to control the instrument. In the 1911A, bits 0, 1, and 15 are the only control bits that are used. To execute a soft reset of the 1911A, the resource manager writes a one (1) to bit 0. If the resource manager writes a one (1) to bit 1 of the control register, the 1911A will not drive the SYSFAIL* line low in response to a system failure. To enable access to A24 address space memory contained inside the 1911A, the resource manager writes a one (1) to bit 15 of the control register. Per the VXIbus specification, the resource manager writes one's to the device dependent bits of the control register whenever it writes to the control register.

Status/Control Register (b+04h)



OFFSET REGISTER FOR A24 (READ/WRITE)

The Offset Register contains the base address of the A24 address space. At power-up the resource manager assigns the 1911A a 2 kbyte block of A24 address space and writes the offset address to the A16 offset address register. This offset address is used when performing reads and writes to the A24 address space.

A16 REGISTERS 08h - 3Fh NOT USED

A24 REGISTERS

The 1911A is controlled by writing information to the internal registers memory mapped to the A24 address space. These registers can be functionally divided up into Trigger Registers, Channel Registers, Control Registers, and Strobe Registers. The memory of the A24 address space is shown in Figure 4-2.

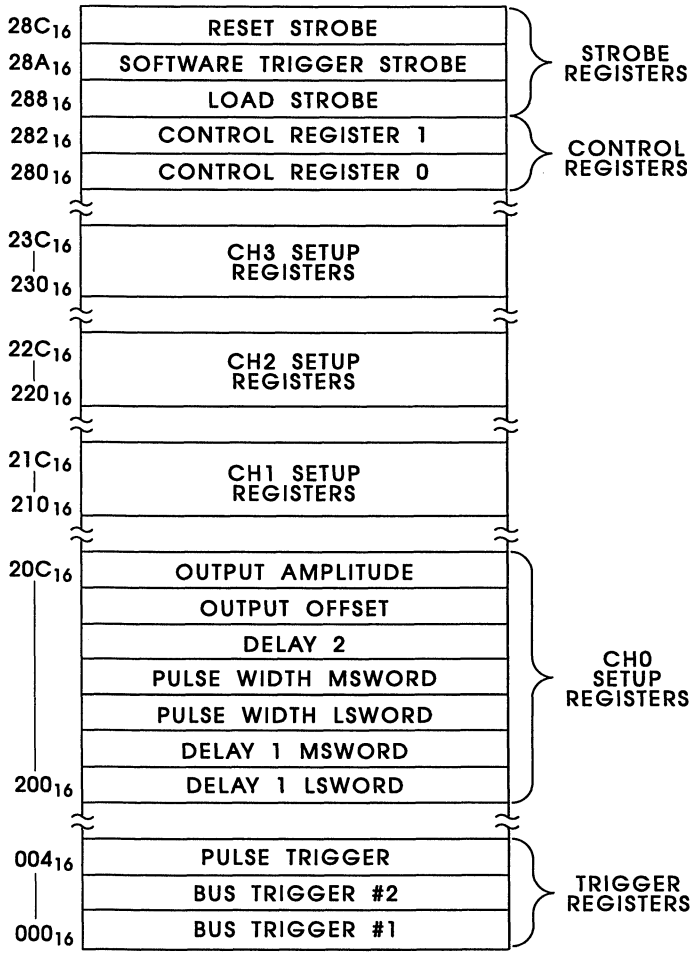


Figure 4-2. A24 Memory Map for 1911A.

TRIGGER CONTROL REGISTERS

The Trigger Control Registers provide routing control of the VXIbus trigger lines TTLTRG(0..7) and ECLTRG(0..1). Using these registers, the 1911A can be programmed to either output to the VXIbus trigger lines or to trigger from the VXIbus trigger lines. The Bus Trigger Registers are used to control signal routing from the 1911A to the VXIbus trigger lines. The Pulse Trigger Registers are used to control triggering of the 1911A from the VXIbus trigger lines.

Bus Trigger Registers (Read/Write)

The Bus Trigger Registers are used to control the routing of a sample of one of the output channels and/or the external trigger input to any of the VXIbus trigger lines. The overall programming model for the VXIbus trigger selection is shown in Figure 4-3.

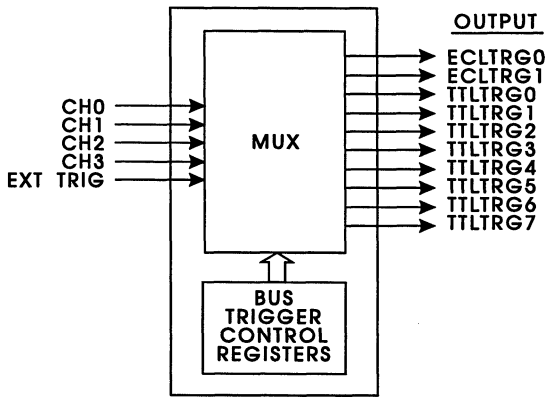


Figure 4-3. Overall Programming Model for Bus Trigger Selection.

Bus Trigger Register 1 is used to route signals to VXIbus trigger lines TTLTRG(0..3) and ECLTRG0. Bus Trigger Register 2 is used to route signals to VXIbus trigger lines TTLTRG(4..7) and ECLTRG1.

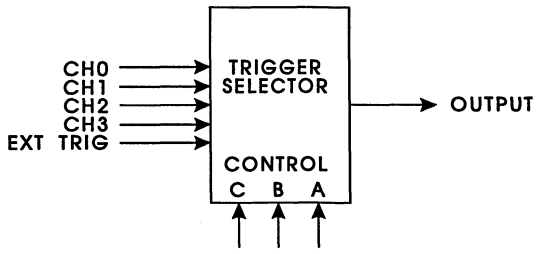
Bus Trigger Register 1 (b+000h)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control		C	B	A	C	B	A	C	B	A	C	B	A	C	B	A
		ECLTRG0			TTLTRG3			TTLTRG2			TTLTRG1			TTLTRG0		

Bus Trigger Register 2 (b+002h)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control		C	B	A	C	B	A	C	B	A	C	B	A	C	B	A
		ECLTRG1			TTLTRG7			TTLTRG6			TTLTRG5			TTLTRG4		

The exact values required for a specific routing are determined by referring to the Bus Trigger Registers shown above and the programming model shown in Figure 4-4.



CONTROL C	B	A	OUTPUT
0	0	0	NOT ASSERTED
0	0	1	CH0
0	1	0	CH1
0	1	1	CH2
1	0	0	CH3
1	0	1	EXT TRIGGER
1	1	0	NOT ASSERTED
1	1	1	NOT ASSERTED

Figure 4-4. Individual Programming Model for Bus Trigger Selection.

For example, to command the 1911A to route a sample of CH0 to the VXIbus TTL Trigger 4 (TTLTRG4), program Bus Trigger Register 2 to make: bit 0 = 1, bit 1 = 0, and bit 2 = 0.

To command the 1911A to route a sample of the external trigger from the front panel input connector on the 1911A to the VXIbus ECL Trigger 0 (ECLTRG0), program Bus Trigger Register 1 to make: bit 12 = 1, bit 13 = 0, and bit 14 = 1

Pulse Trigger Registers (Read/Write)

The Pulse Trigger Registers control the source of triggering for each of the four output channels (CH0, CH1, CH2, and CH3). Each channel can be configured to be triggered from one of the VXIbus trigger lines, the external input trigger, or any of the other channels. The overall programming model for the pulse trigger selection is shown in Figure 4-5.

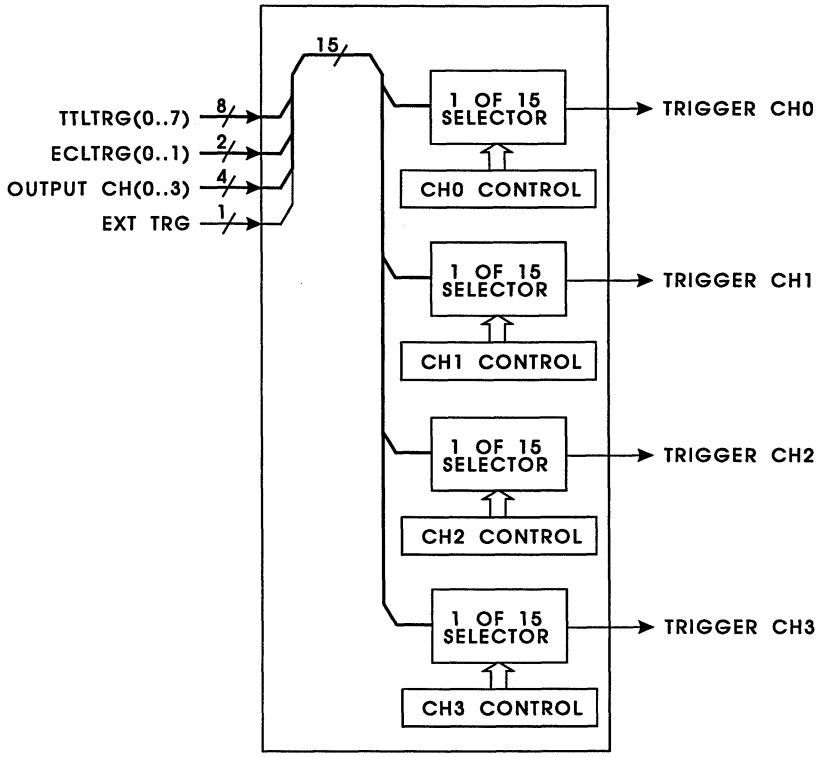
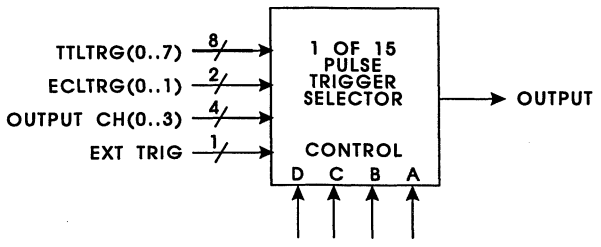


Figure 4-5. Overall Programming Model for PulseTrigger Selection.

Pulse Trigger Register (b+004h)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control	D	C	B	A	D	C	B	A	D	C	B	A	D	C	B	A
	TRIGGER CH3				TRIGGER CH2				TRIGGER CH1				TRIGGER CH0			

Each channel in the 1911A, CH(0..3), can be configured to trigger from one of the 15 trigger sources by writing values to the Pulse Trigger Register. The exact value required for a specific configuration can be determined by referring to the programming model shown in Figure 4-6.



CONTROL D	C	B	A	OUTPUT
0	0	0	0	NOT ASSERTED
0	0	0	1	CH0
0	0	1	0	CH1
0	0	1	1	CH2
0	1	0	0	CH3
0	1	0	1	EXT TRIG
0	1	1	0	TTLTRG0
0	1	1	1	TTLTRG1
1	0	0	0	TTLTRG2
1	0	0	1	TTLTRG3
1	0	1	0	TTLTRG4
1	0	1	1	TTLTRG5
1	1	0	0	TTLTRG6
1	1	0	1	TTLTRG7
1	1	1	0	ECLTRG0
1	1	1	1	ECLTRG1

Figure 4-6. Individual Programming Model for Pulse Trigger Selection.

For example, to command Channel 0 (CH0) of the 1911A to trigger from the VXIbus TTL Trigger 4 (TTLTRG4), program the Pulse Trigger Register to make: bit 0 = 0, bit 1 = 1, bit 2 = 0, and bit 3 = 1.

To command Channel 2 (CH2) of the 1911A to trigger from the external trigger input on the front panel, program the Pulse Trigger Register to make: bit 8 = 1, bit 9 = 0, bit 10 = 1, and bit 11 = 0.

CHANNEL CONTROL REGISTERS (WRITE ONLY)

The Channel Control Registers are used to set delay, pulse width, output amplitude, and offset voltage for each of the four output channels. The 1911A has four sets of channel registers providing independent control over each output channel. These four sets of channel registers are identical except for their memory location.

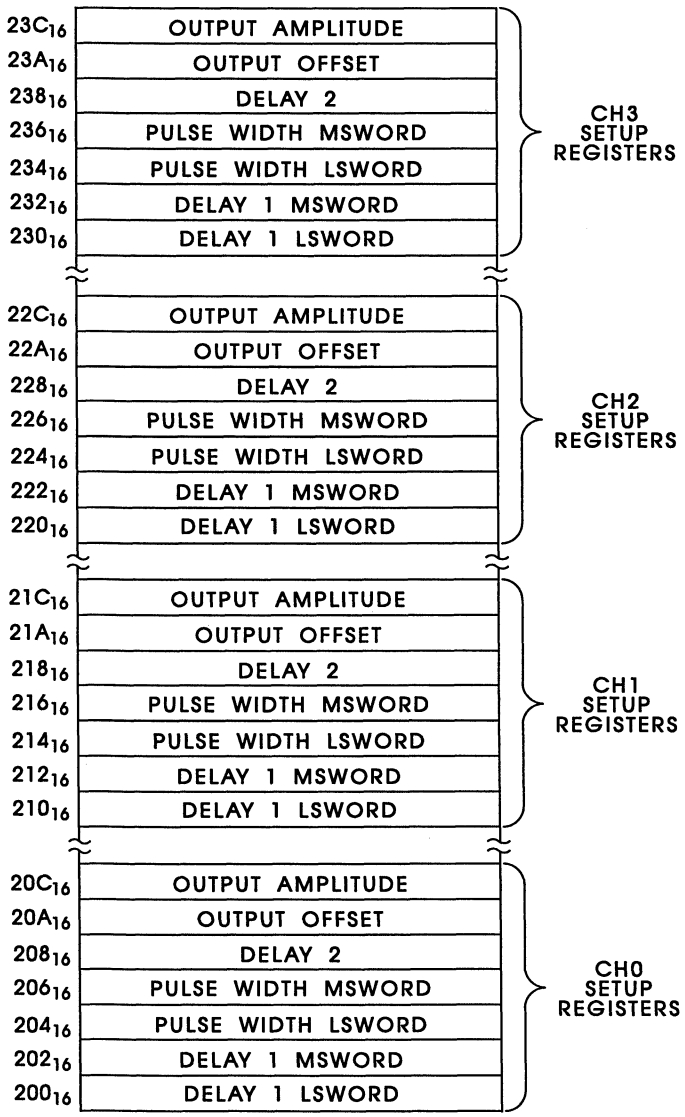


Figure 4-7. Memory Map of Channel Setup Registers.

Writing to a Channel Setup Register does not immediately change the channel parameter. The channel registers are all double buffered which allows the 1911A to be synchronously configured. Each of the channel registers actually consists of two registers—a setup register and a parameter control register. To change a channel parameter, such as output amplitude, a software load strobe must be sent. The load strobe transfers data from the setup register to the parameter control register. The 1911A provides software masking to select which channels will be changed in response to the load strobe. A programming model for Channel Control Registers is shown in Figure 4-8.

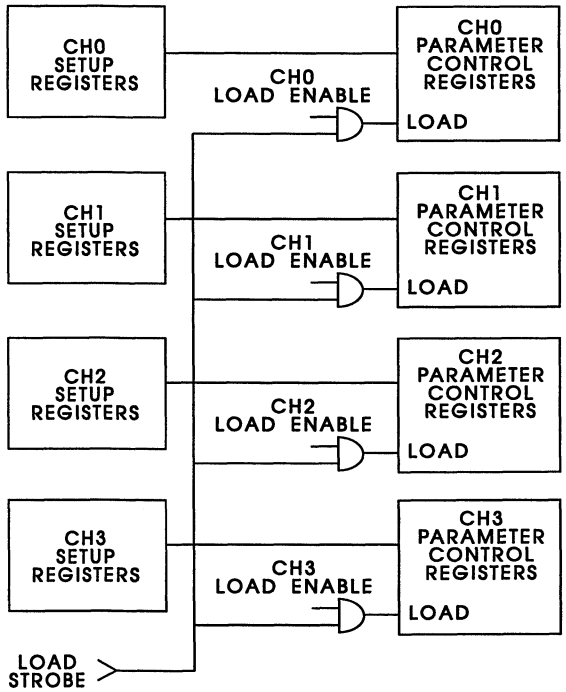


Figure 4-8. Channel Parameter Control Programming Model.

Pulse Delay (Write Only)

For each channel, the 1911A provides a coarse delay (DELAY1) and a fine delay (DELAY2). DELAY1 is 24 bits long and is spread across two 16 bit registers. The first register, for DELAY1, contains the least significant word (LSWORD) and the second register contains the most significant word (MSWORD). The upper 8 bits of the second register (MSWORD) are not used. For DELAY1, the resolution is 50 ns per bit and the minimum delay is 50 ns, so with 24 bits the maximum delay is 838.86 ms (50 ns x 2^{24}). DELAY2 is 6 bits long and has a resolution of 1 ns per bit, so the maximum delay for DELAY2 is 63 ns (1 ns x 2^{6}-1). The total pulse delay is the combination of DELAY1 and DELAY2.

*DELAY1 LSWORD Setup Register (b+2X0h)**

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control																

*DELAY1 MSWORD Setup Register (b+2X2h)**

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control																

Not Used

*DELAY2 Setup Register (b+2X8h)**

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control																
	← Not Used →															

* To program a particular channel, replace the X in the offset address with the desired channel: 0, 1, 2, or 3.

To determine the contents of the register divide the desired delay by 50 ns and program the integer multiple minus 1 into the two DELAY1 registers. Then divide the remainder by 1 ns and program the integer multiple into the DELAY2 register.

For example, to set a pulse delay of 507 ns on Channel 2 (CH2), calculate the required contents of DELAY1 as follows:

INT (507 ns / 50 ns) - 1 = 9 decimal = 0000 0000 0000 0000 0000 1001 binary

MSWORD | LSWORD

DELAY1 LSWORD Setup Register (b+220h)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

DELAY1 MSWORD Setup Register (b+222h)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control									0	0	0	0	0	0	0	0
	← Not Used →															

With 500 ns programmed into DELAY1, this leaves 7 ns, so DELAY2 is programmed to provide the additional 7 ns of delay.

INT (7 ns / 1 ns) = 7 decimal = 00 0111 binary

DELAY2 Setup Register (b+228h)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control											0	0	0	1	1	1
	← Not Used →															

Pulse Width (Write Only)

The 1911A provides two registers for controlling pulse width. The first register contains the least significant word (bits 0 - 15) and the second register contains the most significant word (bits 16 - 23). Combined, the two registers provide 24 bits of control for the pulse width with a resolution of 50 ns per bit and a minimum width of 50 ns. The maximum pulse width is 838.86 ms (50 ns x 2^{24}).

*Pulse Width LSWORD Setup Register (b+2X4h)**

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control																

*Pulse Width MSWORD Setup Register (b+2X6h)**

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control																
	← Not Used →															

* To program a particular channel, replace the X in the offset address with the desired channel: 0, 1, 2, or 3.

To determine the contents of the register, divide the desired pulse width by 50 ns and program the integer multiple minus 1 into the two pulse width registers.

For example, to set a pulse width of 1 µs on Channel 2 (CH2), calculate the required contents of the two pulse width registers as follows:

INT (1µs / 50 ns) - 1 = 19 decimal = 0000 0000 0000 0000 0001 0011 binary

MSWORD | LSWORD

Pulse Width LSWORD Setup Register (b+224h)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1

Pulse Width MSWORD Setup Register (b+226h)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control									0	0	0	0	0	0	0	0
	← Not Used →															

Output Amplitude (Write Only)

The 1911A provides 12 bits of control over output amplitude. The maximum output voltage in Range 0 is 1.05 V p-p (0.256 mV/bit resolution). Selecting Range 1 in the control register will increase the maximum output voltage by a factor of 10 to 10.5 V p-p (2.56 mV/bit resolution).

*Amplitude Setup Register (b+2XCh)**

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control																
	← Not Used →															

* To program a particular channel, replace the X in the offset address with the desired channel: 0, 1, 2, or 3.

To determine the contents of the register, divide the desired output voltage by the resolution of the selected range and program the binary equivalent of the integer value into the Amplitude Setup Register.

For example, to set an output voltage of 0.5 volts on Range 0, calculate the integer value of 0.5 V divided by 0.256 mV and program the binary equivalent of the integer value into the Amplitude Setup Register as follows:

INT (0.5 V / 0.256 mV) = 1953 decimal = 0111 1010 0001 binary

Amplitude Setup Register (b+2XCh)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control					0	1	1	1	1	0	1	0	0	0	0	1
	←Not Used→															

Output Offset (Write Only)

The 1911A provides 12 bits of control over dc offset with a resolution of 2.44 mV per bit. Unlike amplitude, the offset voltage is not affected by changing between Range 0 and 1. The dc offset can be positive or negative over a range of ±5 Vdc.

*Offset Setup Register (b+2XAh)**

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control																
	←Not Used→															

* To program a particular channel, replace the X in the offset address with the desired channel: 0, 1, 2, or 3.

The formula for calculating the offset voltage based on a programmed value is:

$$Vo = 2.44\ mV\ (-2047 + X)$$

where: X is the decimal equivalent of the programmed value.

For example, if bits 0 through 11 of the Offset Setup Register are all 1's, then the DC offset voltage is calculated as follows

1111 1111 1111 binary = 4095 decimal
$Vo = 2.44\ mV\ (-2047 + 4095) \approx 4.997$ Vdc

If bits 0 through 11 of the Offset Setup Register are all 0's, then the dc offset voltage is calculated as follows:

0000 0000 0000 binary = 0 decimal
$Vo = 2.44\ mV\ (-2047 + 0) \approx -4.995$ Vdc

To determine the value to program into the Offset Setup Register, calculate the integer value of the desired output voltage divided by 2.44 mV. Add 2047 to the calculated value and program the binary equivalent into the Offset Setup Register.

For example, to set an offset voltage of 0.25 volts, calculate the integer value of 0.25 V divided by 2.44 mV and program the binary equivalent of the integer value into the Offset Setup Register as follows:

INT (0.25 / 2.44 mV) + 2047 = 103 + 2047 = 2150 decimal = 1000 0110 0110 binary

Offset Setup Register (b+2XAh)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control					1	0	0	0	0	1	1	0	0	1	1	0
	← Not Used →															

CONTROL REGISTERS (WRITE ONLY)

The 1911A contains two 16 bit control registers, Control Register 0 and Control Register 1. These registers, shown below, provide independent control of the four output channels on the 1911A. At power-up, all bits in the control registers are set to zero (o).

Control Register 0 (b+280h)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control																
	CH3	CH2	CH1	CH0	CH3	CH2	CH1	CH0	CH3	CH2	CH1	CH0	CH3	CH2	CH1	CH0
	← RETRIG →				← INVERT →				← RANGE →				← ENABLE →			

Control Register 1 (b+282h)

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control																
	← Not Used →				CH3	CH2	CH1	CH0	CH3	CH2	CH1	CH0	CH3	CH2	CH1	CH0
					← RESET →				← SWTRIG →				← LOAD →			

The purpose of each of the seven parameters, for each channel, are described below. The first four parameters (ENABLE, RANGE, INVERT, and RETRIG) are direct. Writing to one of these bits causes an event to occur immediately. The second three parameters (LOAD, SWTRIG, and RESET) are masks. LOAD and SWTRIG are active high and RESET is active low; therefore, writing a one (1) to a LOAD or SWTRIG bit, or a zero (0) to a RESET bit, enables an event to occur.

For example, if the RESET bit for Channel 2 is a zero (0) and the RESET bits for the other three channels are set to one (1), then writing to the Reset Strobe address will cause both the Channel Setup Registers and the Channel Parameter Control Registers for CH2 to be cleared, but will not affect the registers for CH1, CH3 or CH4.

ENABLE: A one (1) in this bit connects the output from the particular channel to the front panel connector. A zero (0) terminates the output into an internal 50 Ω load.

RANGE: High/Low Range select. A one (1) in this bit increases the output amplitude from the channel by a factor of 10. Range does not affect offset voltage.

INVERT: A one (1) in this bit causes the output from the particular channel to be inverted.

RETRIG: A one (1) in this bit causes the 1911A to automatically retrigger at the end of a pulse. This allows a channel to freerun, continuously generating pulses.

Note: Prior to setting this bit high, the particular channel must be setup and data loaded using the load strobe.

LOAD: The LOAD bits are active high enable bits. If the LOAD bit for a particular channel is high then writing to the Load Strobe address will load the Channel Parameter Control Registers synchronously activating all data previously written to the Channel Setup Registers.

SWTRIG: The SWTRIG bits are active high enable bits. Writing to the Software Trigger Strobe address will trigger all channels with a one (1) in the SWTRIG enable bit.

RESET: The RESET bits are active low enable bits. Writing to the Reset Strobe address will clear the Channel Setup Registers and the Channel Parameter Control Registers for all channels with zero's (0's) in the RESET enable bit.

STROBE REGISTERS (WRITE ONLY)

The 1911A has three strobe registers. Writing to the address of a strobe register will cause an event to occur. Specific information on each of the three strobe registers is covered below.

Load Strobe (b+288h)

A write to this address transfers new data to each channel selected by the LOAD enable mask bits (Bits 0..3 of Control Register 1). This strobe transfers the data from the enabled Channel Setup Registers to the corresponding Channel Parameter Control Registers synchronously activating the data previously written to the Channel Setup Registers.

Software Trigger Strobe (b+28Ah)

A write to this address sends a trigger pulse to the channels selected by the SWTRIG mask bits in Control Register 1.

Reset Strobe (b+28Ch)

A write to this address resets the channels selected by the RESET trigger mask in Control Register 1 causing zeros to be written to the Channel Setup Registers and the corresponding Channel Parameter Control Registers.

PROGRAMMING EXAMPLE

In this example the 1911A will be programmed to output a continuous pulse train on Channel 0. The pulse train is to have a 50 ns pulse width, with a frequency of 1 MHz. The pulse will be 5.25 volts into 50 ohms with an offset of 0 volts, as shown in Figure 4-9.

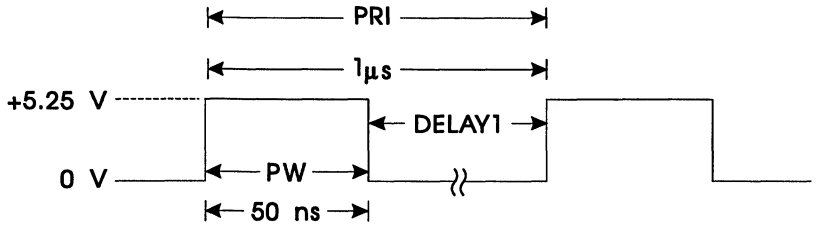


Figure 4-9. CH0 Output Signal.

To set up the output as shown above, the following data should be written to the 1911A:

DESCRIPTION	A24 ADDRESS (hex)	DATA(hex)
CH0 DELAY1 LSWORD	Base + 200	0012
CH0 DELAY1 MSWORD	Base + 202	0000
CH0 Pulse Width LSWORD	Base + 204	0000
CH0 Pulse Width MSWORD	Base + 206	0000
CH0 DELAY2	Base + 208	XX00
CH0 Output Offset	Base + 20A	X7FF
CH0 Output Amplitude	Base + 20C	XFFF
Control Register 1	Base + 282	XE01
Load Strobe	Base + 288	XXXX
Control Register 0	Base + 280	1011
where X = don't care		

The frequency is set using the DELAY1 Registers at A24 offset addresses 200h and 202h. In the freerun state, this is the "delay" time from the end of one pulse until the beginning of the next pulse (PRI - PW). The Pulse Width Registers at A24 offset addresses 204h and 206h are set to zero. This sets the output pulse width to the minimum value of 50 ns. The DELAY 2 Register is set to zero because the desired delay is an exact integer multiple of 50 ns. The Output Offset Register is set to one-half of full scale setting the dc offset to zero (0) volts. The Output Amplitude Register is set to full scale. Control Register 1 is configured to allow resetting of Channel 0 (reset is active low) and to enable the loading of Channel 0 Parameter Control Registers. After setting up Control Register 1 to enable loading the data, a Load Strobe is sent by writing to the strobe address. Writing to a Load Strobe address transfers the setup data to the Parameter Control Registers. The actual data used when writing to the Load Strobe address has no meaning which is the reason that the data word sent to the strobe address is shown as a "don't care". Control Register 0 is configured to enable Channel 0 Retrigger Enable and Channel Enable as well as selecting Range 1 for Channel 0.

Note: The Channel 0 Retrigger Enable must be set after loading the Channel 0 Parameter Control Registers.

Once the channel is freerunning, the pulse parameters can be changed by first writing to the Channel Setup Register, and then writing to the Load Strobe (assuming that the Load Enable has not been deactivated). If the channel is reset, the Retrigger Enable must be de-asserted, the channel parameters set up, loaded, and then the Retrigger Enable reactivated.

Next, the signal from Channel 0 will be used to trigger Channel 1. For this example, Channel 1 will be set up to output a 100 ns pulse delayed from the Channel 0 trigger by 155 ns. The minimum channel-to-channel delay is specified at 100 ns. This means that it takes at least 100 ns for a trigger from one channel to cause a change on the output of another channel. Of this 100 ns minimum delay, 50 ns comes from the triggering circuits and the other 50 ns is the minimum delay of the DELAY1 Register. For this example, the amplitude for the output pulse from Channel 1 will be set to 2.63 volts peak-to-peak into 50 ohms with a dc offset of 2.5 volts, as shown in Figure 4-10.

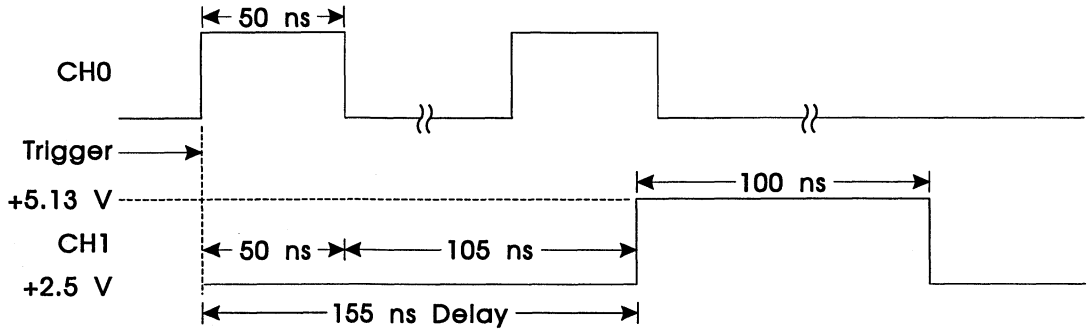


Figure 4-10. CH1 Output Signal.

To set up the 1911A as described, program the instrument with the following data:

DESCRIPTION	A24 ADDRESS (hex)	D A T A (hex)
CH1 DELAY1 LSWORD	Base + 210	0001
CH1 DELAY1 MSWORD	Base + 212	0000
CH1 Pulse Width LSWORD	Base + 214	0001
CH1 Pulse Width MSWORD	Base + 216	0000
CH1 DELAY2	Base + 218	XX05
CH1 Output Offset	Base + 21A	XFFF
CH1 Output Amplitude	Base + 21C	X7FF
Control Register 1	Base + 282	XC02
Load Strobe	Base + 288	XXXX
Control Register 0	Base + 280	1033
Pulse Trigger	Base + 004	0010
where X = don't care		

In this example, the DELAY1 Register is programmed for a 100 ns delay. This 100 ns plus the internal 50 ns delay caused by the triggering circuits means that the total delay is 150 ns, so an additional 5 ns is required. This additional delay will be programmed into the DELAY2 Register. The minimum setable pulse width for the 1911A is 50 ns, so if the Pulse Width Registers are loaded with all zeros (0), the pulse width would be 50 ns. To set a pulse width of 100 ns, the Pulse Width Registers are programmed for one 50 ns increment above the minimum pulse width of 50 ns. The Offset Register is programmed for the maximum positive dc offset—2.5 volts into 50 Ω. The Output Amplitude Register is programmed to one-half of full scale setting the peak-to-peak amplitude of the pulse at 2.63 volts (5.25 / 2) into 50 Ω. Control Register 1 is set up to allow a reset of Channel 0 and Channel 1 and to allow loading of Channel 1 parameters (the load enable for Channel 0 was deactivated to prevent accidental changes of Channel 0 parameters). The write to the Load Strobe was to load Channel 1 parameters. Control Register 0 was configured to keep Retrigger Enable active for Channel 0, set the Range to 1 for Channel 0 and Channel 1, and enable Channel 0 and Channel 1. Finally, the Pulse Trigger register is configured to produce a Channel 1 Trigger from an internal Channel 0 signal.

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